# **Faculty Profile**

Name Mr. Satish Sudhakar Narkhede

Designation Associate Professor

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## **Educational Qualifications**

Degree	University/Institution	Year of Passing
Ph.D.	SPPU	2016
ME (Elex Engg)	SPPU	2000
BE (Ind. Elex. Engg)	SSGMCE, Shegaon	1988

### **Professional Experience**

Sr. No.	Designation & Institute	Duration
1	Lecturer	01/07/1994 to 31/07/2000
2	Assistant Professor	01/08/2000 to 30/06/2011
3	Associate Professor	01/07/2011 to 31/08/2024
	Re-Employment as Asso. Prof	04/09/2024 till date

#### **Research Publications**

Sr. No.	Title	Publication/Conference
1	Arundhati S. Dhampalwar, Mr. S. S. Narkhede," A System on a chip FIR Filter using Partial Reconfiguration Platform"	NCNTE-2010, at Fr. C. Rodrigues Institute of Technology, Thane, 20-21 Jan 2010.
2	Yogita Azar, S.S Narkhede "System on chip FIR filter using partial Reconfiguration platform" Feb 2010, Father C Rodrigues Institute of Technology washi	National conference on nascent technology, 2010
3	Yogita Azar, S.S Narkhede, "Partial reconfiguration of FPGA at run time"	National conference on pervasive computing 2010

4	Yogita Azar, S.S Narkhede, "Dynamic partial reconfiguration of FPGA, used in matrix multi for area and time efficiency,	National conference on pervasive computing 2010
5	Arundhati S. Dhampalwar, Mr. S. S. Narkhede," A SOC for Matrix Inversion Using Dynamic Partial Reconfiguration of FPGA"	NCPC-2010, at Sinhgad College of Engineering, Vadgaon Pune,9-10 APR 2010
6	Anumeha Zanjal and S.S Narkhede, "Design and Frabrication of Fractal Shaped Microstrip Band Pass Filter (Synthetic Aperture Radar Application)"	National Conference on Sensor Networks and Embedded Systems (NCSNES-2011), Abasaheb Garware College, Pune
7	Anumeha Zanjal and S.S Narkhede, "Design and Fabrication of Fractal Shaped Microstrip Band Pass Filter (Synthetic Aperture Radar Application)"	ePGCON-April 2011, MIT Pune.
8	Arundhati S. Dhampalwar, Mr. S. S. Narkhede, "A reconfigurable digital filter based on partial reconfiguration of FPGA,"	iCost 2011 International Conference On Sunrise Technologies at SSVPS B. S. Deore College of Engineering Post Vidyanagri, Dhule, Maharashtra, 13-15 Jan 2011.
9	Arundhati S. Dhampalwar, Mr. S. S. Narkhede, "A Reconfigurable FIR Filter Design Using DPR Of FPGA,"	ICSSA-2011 at G. H. Patel College of Engineering & Technology, Vallabh Vidhyanagar., Anand, Gujarat pp.118, 24-25 Jan,2011.
10	Rohit Bodhe, Satish Narkhede, Shirish Joshi, "Design of Simulink Model for OFDM and Comparison of FFT-OFDM AND DWT- OFDM".	International Journal of Engineering Science and Technology (IJEST), ISSN: 0975-5462, Vol. 4 No.5, Pages-1914-1924, 05 May 2012
11	Rohit Bodhe, Shirish Joshi, Satish Narkhede, "Performance Comparison of FFT and DWT based OFDM and Selection of Mother Wavelet for OFDM"	International Journal of Computer Science and Information Technologies (IJCSIT), ISSN: 0975- 9646,Vol. 3 No.3, Pages- 3993-3997, 2012

12	G. V. Chaudhari, S. S. Narkhede, "Desing of DGS microstrip antenna with Array structure ground plane"	ePGCON2012, Pune.
13	Samruddha Thakur, S. S. Narkhede, Tapas Bhuiya, "Microstrip patch antenna array for Rainfall RADAR", 2013	Fourth International Conference on Computing, Communications and Networking Technologies (ICCCNT), Publisher-IEEE
14	Satish Narkhede, Gajanan Kharate, Bharat Chaudhari, "Design and Implementation of an Efficient Instruction Set for Ternary Processor"	International Journal of Computer Applications, Volume-83, issue-16, Publisher-Foundation of Computer Science16 December 2013
15	Arundhati S. Dhampalwar, Mr. S. S. Narkhede, "A reconfigurable digital filter based on partial reconfiguration of FPGA,"	iCost 2011 International Conference On Sunrise Technologies at SSVPS B. S. Deore College of Engineering Post Vidyanagri, Dhule, Maharashtra, 13-15 Jan 2011.
16	A. P. Dhande, Satish S. Narkhede, Shridhar S. Dudam, "VLSI Implementation of ternary gates using Tanner tool", 2014	2nd International Conference on Devices, Circuits and Systems (ICDCS), Publisher-IEEE, pp1-5, 6–8 March 2014,
17	Sutaria Jimmy, Satish Narkhede, "Design of ternary D latch using carbon nano tube field effect transistors",2015	2nd International Conference on Electronics and Communication Systems (ICECS), Publisher-IEEE, pp151- 154, 26–27 February 2015
18	Perni Venu Gopal, Satish Narkhede, G Sasikala, "Implementation of ternary logic gates using FGMOS",2015	international conference on smart technologies and management for computing, communication, controls, energy and materials (ICSTM), Publisher-IEEE, pp. 275-279, 6–8 May 2015
19	SS Narkhede, BS Chaudhari, GK Kharate, "A Novel MIFGMOS Transistor based Approach for the Realization of ternary gates"	ICTACT Journal on Microelectronics, Volume- 1, issue-2, Publisher- Foundation of Computer Science

20	Siddharth H Pethe, Satish Narkhede,	IOSR Journal of VLSI and
	"Design of Ternary D Flip-Flop Using	Signal Processing (IOSR-
	Neuron MOSFET"	JVSP) Volume, Volume-5, issue-2,Publisher-
		Foundation of Computer
		Science
21	Makani Nailesh, Satish Narkhede, "Design	Published in 2016
	of ternary FinFET SRAM Cell"	Symposium on colossal Data Analysis and
		Networking (CDAN),
		Publisher-IEEE, pp1-5, 18-
		19 March 2016
22	Kushawaha Jyoti, Satish Narkhede, "A approach to ternary logic gates using	AICTC '16: Proceedings of the International
	FinFET"	Conference on Advances in
		Information
		Communication
		Technology & Computing, Article No-59 , pp1-6,
		December 2016
23	Makani Nailesh Kishor, Satish S Narkhede,	ICTACT Journal on
	"A Novel Finfet Based Approach For The	Microelectronics, Volume-
	Realization Of Ternary Gates"	2, issue-2, Publisher- Foundation of Computer
		Science, pp 254-260, ISSN
		23951672
24	Aonkar B Takalikar, S S Narkhede, "Design	ICTACT Journal on
	and Simulation of a 10 GSPS Low Power	Microelectronics, Volume- 3, issue-2, Publisher-
	Sample and Hold Less Analog to Digital Converter Using Carbon Nanotube Field	ICTACT, pp 404-410,
	Effect Transistors".	ISSN: 23951672, Year-
		2017
25	S. S. Narkhede, Nikita Nikam, "Design and	ICTACT Journal on Microelectronics, Volume-
	Analysis of leaky wave antenna to generate the Bessel Beam".	5, issue-2, Publisher-
		ICTACT, pp 793-799,
		ISSN: 2395-1680 (online),
		July 2019

#### **Books Published**

Sr. No.	Title	Publisher & Year
	NIL	

## **Conferences / Seminars Attended**

Sr. No.	Conference/Seminar	Year
	NII	

## Awards & Recognitions

	17
,	Year
Torchbearer of Education Award 2020 for leading	2020
the students towards light in tough times by Coding	
Ninjas.	
Golden Aim Award for Excellence & Leadership in	2022
Education - most innovative TPO.	
Certificate of appreciation for colossal contribution	2022
towards improving the employability ecosystem &	
guiding students towards a brighter future by SHL.	
Certificate of appreciation by ZS Associate for	2022
ongoing support and contribution in organizing	
placement initiatives for ZS at your campus to	
sustain this relationship with the institute.	
Certificate of appreciation by Atos for hosting on the	2022
campus for the Campus Placement Program for	
2022 batch to recognize your distinguished	
contribution in organizing the placement activities	
and continued cooperation between Pune Institute	
of Computer Technology and Atos, creating bright	
career opportunities for your students and alumni.	
	<ul> <li>Ninjas.</li> <li>Golden Aim Award for Excellence &amp; Leadership in Education - most innovative TPO.</li> <li>Certificate of appreciation for colossal contribution towards improving the employability ecosystem &amp; guiding students towards a brighter future by SHL.</li> <li>Certificate of appreciation by ZS Associate for ongoing support and contribution in organizing placement initiatives for ZS at your campus to sustain this relationship with the institute.</li> <li>Certificate of appreciation by Atos for hosting on the campus for the Campus Placement Program for 2022 batch to recognize your distinguished contribution in organizing the placement activities and continued cooperation between Pune Institute of Computer Technology and Atos, creating bright</li> </ul>

## **Areas of Interest**

Sr. No.	Area
1	Analog Circuits
2	Integrated design
3	Multivalued logic